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Electrical & Computer Engineering

"MAKE COMPUTING SCALABLE, FAST, AND SECURE"

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TIME: 3:30 PM – 5:00 PM
ENGINEERING CENTER
ROOM EC 3753
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MIAMI, FL 33174

Abstract: As vendors are putting more and more cores into a single processor, the traditional cache-based memory hierarchy and bus-oriented communication architecture will have the scalability issue and need to be replaced. In the first part of this talk, I will present the prototype of a tool chain that takes an application written in OpenCL and generates the optimal heterogeneous manycore platform and the corresponding software running on the platform for embedded system applications. The efficient memory hierarchy and the adaptive network-on-chip are used as building infrastructure of the generated manycore platform.

As single processor becomes parallel, the traditionally homogeneous high-performance computers, i.e., supercomputers, are becoming heterogeneous. Hardware accelerators, such as Field-Programmable Gate Arrarys (FPGAs), Graphics Processing Units (GPUs), and Intel Many Integrated Core (MIC) Architectures, are brought in to deal with the "power wall" in supercomputing. In the second part of this talk, I will use benchmarks to demonstrate the potential of performance improvement for using hardware accelerators. I will also discuss the challenges and solutions to deploy applications on supercomputers with hybrid nodes.

The third part of the talk presents my investigation of physically unclonable functions (PUFs) in hardware. PUF basically is a special hardware circuit that generates a response as the output if a challenge is applied as the input. Given the same challenge, the PUFs on different devices should generate completely different responses due to manufacturing variations. The unique PUF output can be used as hardware fingerprint or DNA for authentication purpose. I will introduce the state of the art of PUF research and present a novel PUF design using a chain of multiplexers.

Biography: Miaoqing Huang is an Assistant Professor at the Department of Computer Science and Computer Engineering, University of Arkansas since January 2010. He obtained a PhD degree in Computer Engineering from The George Washington University in August 2009 and a BS degree in Electrical Engineering from Fudan University in July 1998, respectively. His research interests include heterogeneous manycore architecture, high-performance computing with hardware accelerators, and hardware-oriented security. He has close to 50 publications at various venues including IEEE TC, IEEE TPDS, FCCM, FPL, FPT. He is a member of IEEE.

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