



Seminar Experience

ELECTRICAL & COMPUTER ENGINEERING

Friday, April 10

FIU Engineering Center

11:00 am—12:00 pm

EC Room # 1105

www.ece.fiu.edu



“Coping with delay defects in deep submicron digital integrated circuits”

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ABSTRACT

Testing for delay defects is increasingly challenging in digital integrated circuits. Complex fault models must be used for the generation of input stimuli. Scalable automatic test pattern generation methods are presented. This presentation also outlines approaches that identify the location of embedded delay defects.

BIOGRAPHY

Spyros Tragoudas (BSc 1986, MSc 1988, PhD 1991) is Professor and Department Chair at the Electrical and Computer Engineering (ECE) Department, Southern Illinois University at Carbondale (SIUC), and the Director of the National Science Foundation (NSF) Industry University Cooperative Research Center (IUCRC) on Embedded Systems at the SIUC site. He has held prior appointments with the faculty of the ECE Department at the University of Arizona, and with the faculty of the Computer Science Dept. at SIUC.

His current research interests are in the areas of VLSI Design and Test Automation and embedded systems. Dr. Tragoudas has published over two hundred papers in journals and peer-reviewed conference proceedings in these areas, and has received three outstanding paper awards for research in VLSI Testing. His research has been funded from federal agencies and industry. He has served and current serving on the editorial board of several journals, the technical program committees of many conferences, was the program chair of the DFTS'09, and the general chair of DFTS'10.